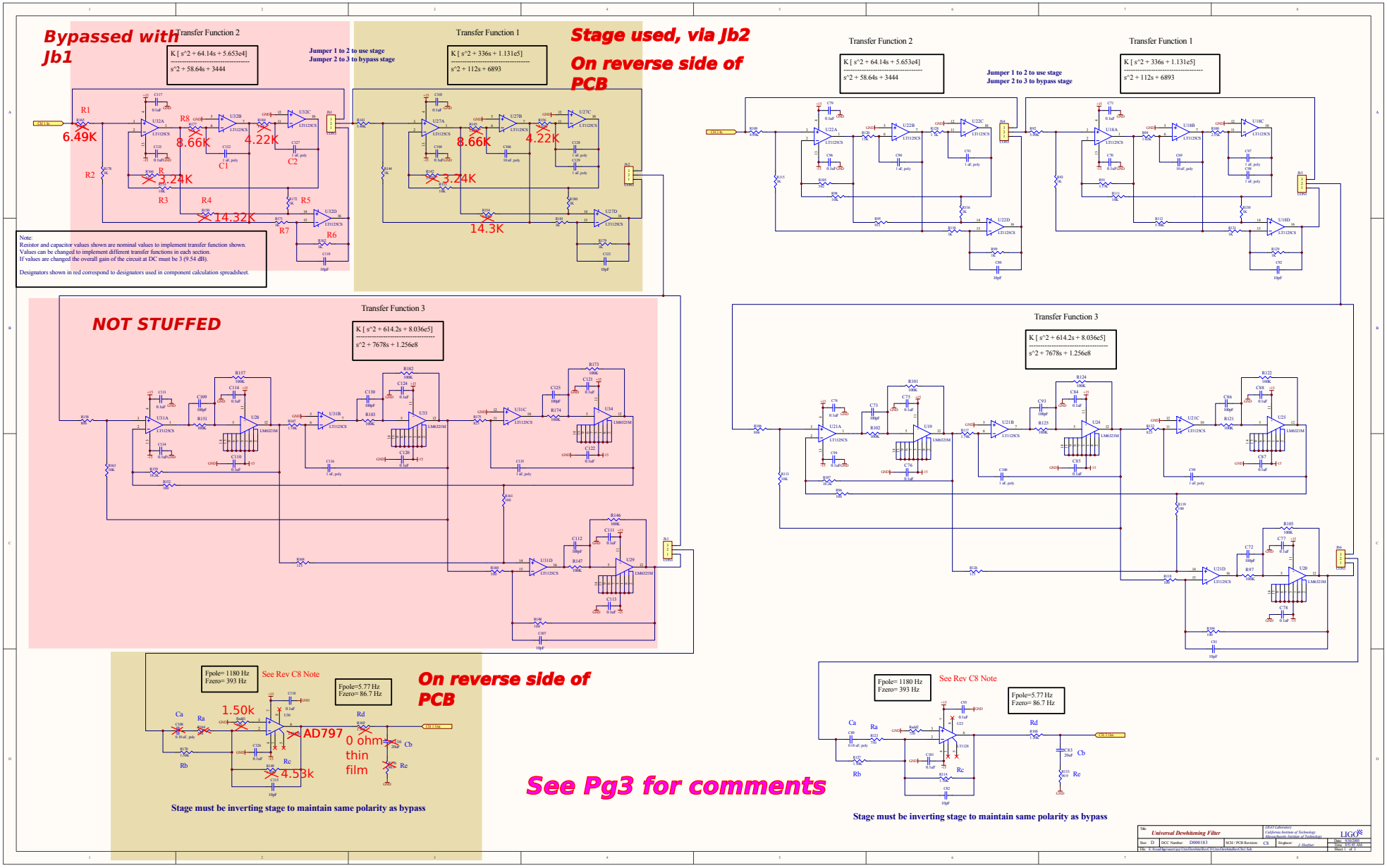
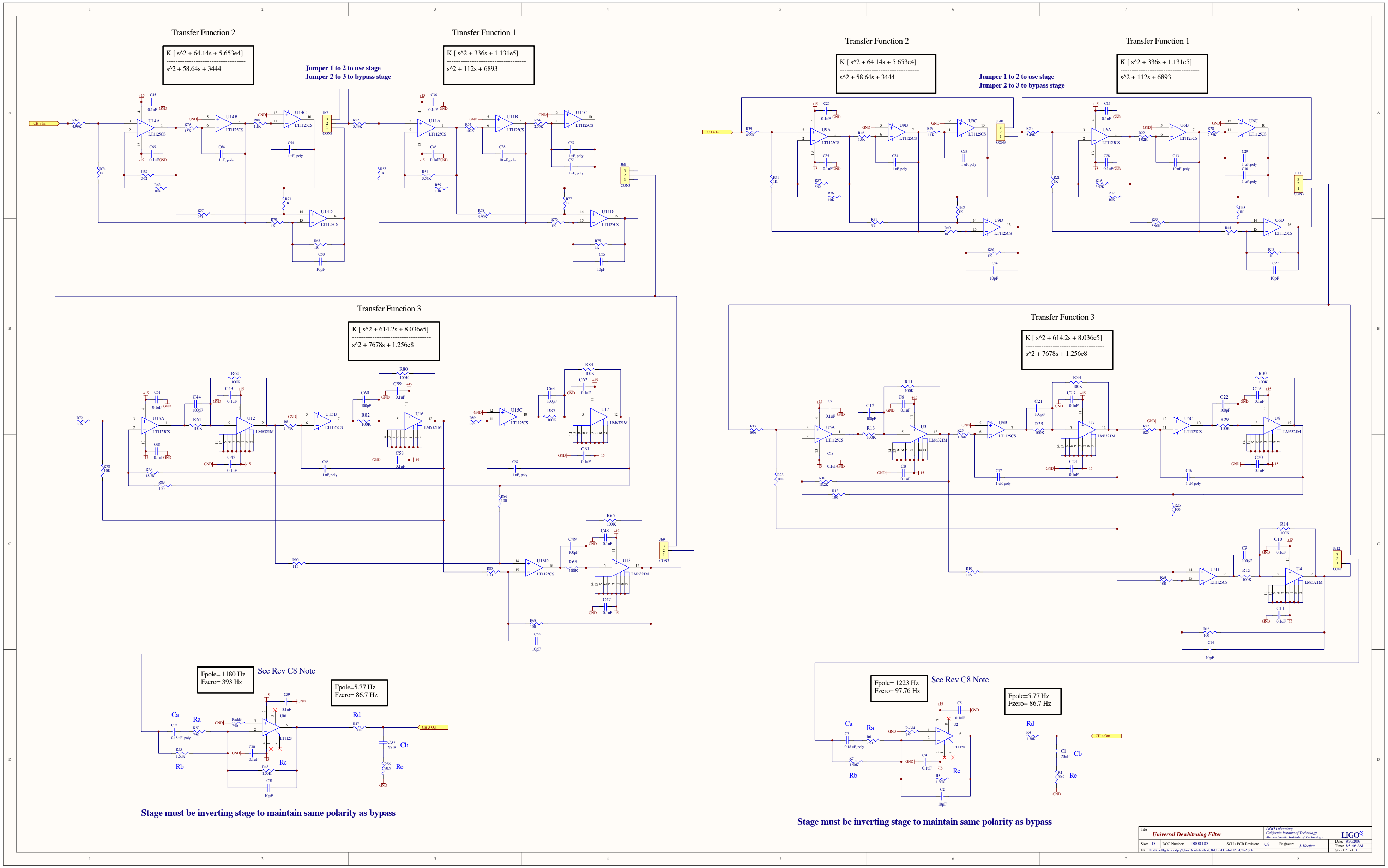

Bypassed with Jb1
Transfer Function 2
K [s^2 + 64.14s + 5.653e4]
s^2 + 58.64s + 3444
Jumper 1 to 2 to use stage
Jumper 2 to 3 to bypass stage
Transfer Function 1
K [s^2 + 336s + 1.131e5]
s^2 + 112s + 6893
Stage used, via Jb2
On reverse side of PCB
R1
6.49K
R8
8.66K
4.22K
C1
C2
R2
3.24K
R3
R4
14.32K
R7
R6
R5
8.66K
4.22K
3.24K
14.3K
Note:
Resistor and capacitor values shown are nominal values to implement transfer function shown.
Values can be changed to implement different transfer functions in each section.
If values are changed the overall gain of the circuit at DC must be 3 (9.54 dB).
Designators shown in red correspond to designators used in component calculation spreadsheet.
NOT STUFFED
Transfer Function 3
K [s^2 + 614.2s + 8.036e5]
s^2 + 7678s + 1.256e8
Fpole= 1180 Hz
Fzero= 393 Hz
See Rev C8 Note
Fpole=5.77 Hz
Fzero= 86.7 Hz
On reverse side of PCB
1.50k
AD797
0 ohm
thin
film
4.53k
Ca
Ra
Rb
Rc
Rd
Cb
Re
Stage must be inverting stage to maintain same polarity as bypass
See Pg3 for comments
Universal Deshitening Filter
LIGO



Transfer Function 2
K [s^2 + 64.14s + 5.653e4]
s^2 + 58.64s + 3444
Transfer Function 1
K [s^2 + 336s + 1.131e5]
s^2 + 112s + 6893
Jumper 1 to 2 to use stage
Jumper 2 to 3 to bypass stage
Transfer Function 3
K [s^2 + 614.2s + 8.036e5]
s^2 + 7678s + 1.256e8
Fpole= 1180 Hz
Fzero= 393 Hz
See Rev C8 Note
Fpole=5.77 Hz
Fzero= 86.7 Hz
Ca
Ra
Rb
Rc
Rd
Cb
Re
Stage must be inverting stage to maintain same polarity as bypass
Transfer Function 2
K [s^2 + 64.14s + 5.653e4]
s^2 + 58.64s + 3444
Transfer Function 1
K [s^2 + 336s + 1.131e5]
s^2 + 112s + 6893
Jumper 1 to 2 to use stage
Jumper 2 to 3 to bypass stage
Transfer Function 3
K [s^2 + 614.2s + 8.036e5]
s^2 + 7678s + 1.256e8
Fpole= 1223 Hz
Fzero= 97.76 Hz
See Rev C8 Note
Fpole=5.77 Hz
Fzero= 86.7 Hz
Ca
Ra
Rb
Rc
Rd
Cb
Re
Stage must be inverting stage to maintain same polarity as bypass
Title
Universal Dewhitening Filter
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
LIGO
Size: D
DCC Number: D000183
SCH / PCB Revision: C8
Engineer: J. Heefner
Date: 9/30/2003
Time: 8:51:46 AM
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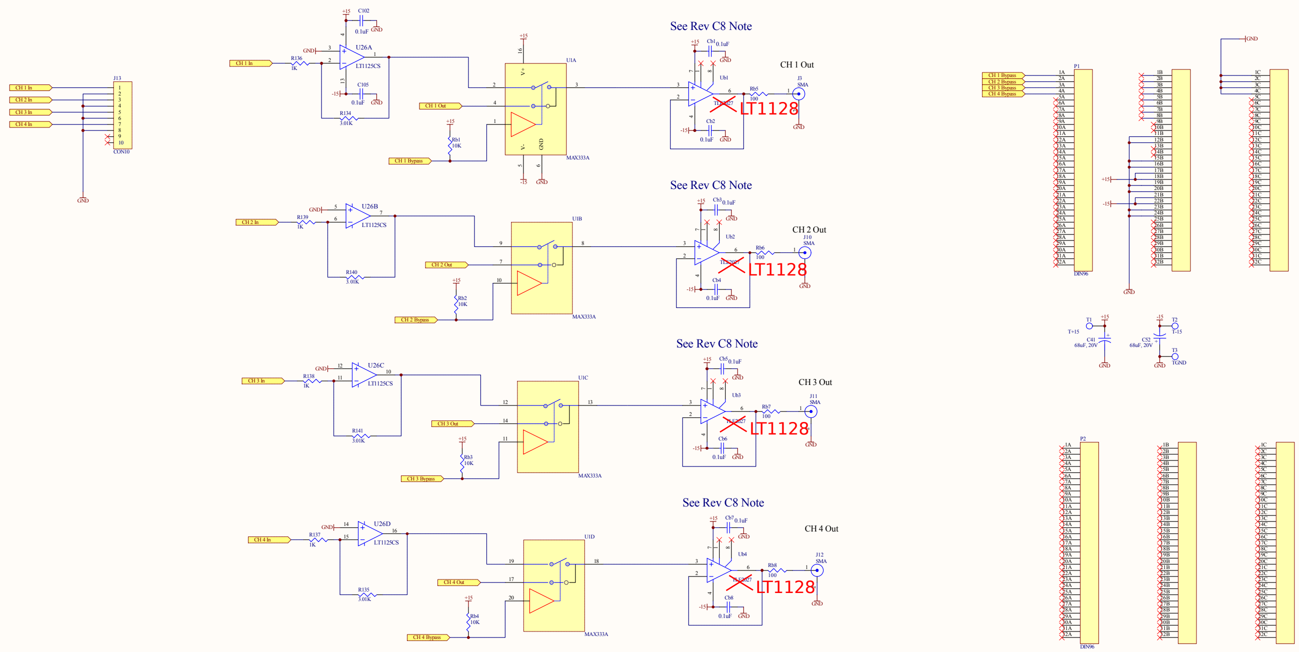
Sheet 2 of 3



Comments:
1. D000183 Rev C, S/N B5172, labelled "B5", used for 40m SRM
2. Deviations from schematic marked in **RED**
3. Only one channel was checked, I assume that all 4 channels are identical

Proposed changes:
1. Get rid of DC gain of 3 (change R134, R140, R141, R135 from 3.01k to 1k, and R149, R114, R48, R5 from 4.53k to 1.5k)
2. Change critical resistors from thick-film to thin film

Revision	Description of Change	Date
A	Initial release	5/00
A1	1. Added note about RevA1 upgrade board. 2. Changed R134, R135, R140, R141 to 3.01K	1/01
B	1. Added jumpers JbX to selectively jumper individual filter sections. 2. Added output buffer amps UbX to each channel. 3. All components added for Rev B have a "b" in the designator. 4. Removed output jumpers J1, J2, J4, J5, J6, J7, J8, J9. 5. Added test points for power connection.	3/01
B1/B2	1. Changed componet values to have two sections w/ 2 ea butterworth poles at 30 Hz and 2 ea. butterworth zeros at 100 Hz to allow for easier lock acquisition of IFO.	4/01
B3	1. Changed AD829 to LT1128 or OP27 (Ub1, Ub2, Ub3, Ub4) 2. Changed components to make 2 poles @ 15Hz, 2 zeros @ 75Hz.	6/02
B4	1. Changed R4, R47, R108, R169 to 158K. 2. Changed C1, C37, C83, C116 to 10uF. 3. Changed R1, R56, R133, R176 to 3.16K. This puts a 0.1 Hz pole and 5 Hz zero in the output of each channel.	7/02
B5	1. Rev B5 is a change to Rev B3 with poles at 15Hz and zeros at 100Hz. 2. Changed R69, R52, R39, R20, R165, R143, R109, R92 to 6.49K 3. Changed R67, R51, R37, R19, R166, R142, R105, R91 to 3.24K 4. Changed R79, R54, R46, R22, R177, R145, R120, R94 to 8.66K 5. Changed R88, R64, R49, R28, R184, R156, R128, R100 to 4.22K 6. Changed R57, R58, R31, R33, R150, R154, R95, R112 to 14.3K	9/02
B6	Rev B6 On some channels the values in the output stages have been changed to the following: Ra = 2.37K Rb = 23.7K Rc = 71.5K Rd = 22K Re = 3.24K Ca = 0.22uF Cb = 1 uF This adds poles at 7Hz, and 3.05KHz and zeros at 50Hz and 305Hz with a DC gain of 9.6dB.	1/03
B7	1. Rev B7 has two sections each with poles @ 7 and 7Hz, zero at 50 and 50 Hz. The output stage has a DC gain of 3 with a zero at 250 Hz and pole at 2500 Hz. 2. This revision of the module is used for the MC2 output at LLO and the 40 Meter.	2/03
C	1. Radd1, Radd2, Radd3, Radd4 added to rev C design to cancel offsets observed on final stage. Resistor values chosen to null output offset. 2. All Rev B notes apply to Rev C schematics.	2/03
C8	1. Values changed to give Rev A1 transfer function with modified real pole and zero on output stage as shown. 2. Output op amp changed from AD829 to TLE2027 for stability. It may be an SO-8 package in a socket adapter. 3. All Rev B notes apply to Rev C schematics.	9/03

Title: Universal Dewhitening Filter		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	LIGO
Size: D	DCC Number: D000183	SCH / PCB Revision: C8	Engineer: J. Heefner
File: E:\h\cad\ligo\users\jay\UnivDewhite\RevC8\UnivDewhiteRevC8s3.Sch		Date: 9/30/2003 Time: 8:51:46 AM	Sheet 3 of 3