Phase Noise in Digital Frequency Dividers

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***Abstract*—This paper presents a physical derivation of phase noise in source-coupled-logic frequency dividers. This analysis takes into account both white and flicker noise sources and is verified on two 32/33 dual-modulus prescalers integrated in a 0.35-μm CMOS process. Design techniques for high-speed and low-noise operation are provided. The two integrated prescalers are identical apart from a synchronizing flip-flop at the output of one of them. The measured phase spectra are in good agreement with the estimates and demonstrate that the final synchronization allows a better trade-off between noise and power consumption. The maximum operating frequency is 3 GHz, the power consumption is 27 mW and the phase noise floor is −163 dBc/Hz referred to the 78-MHz output.**

***Index Terms*—CMOS integrated circuit, frequency dividers, frequency synthesizer, jitter, phase noise, phase-locked loops (PLLs).**

I. Introduction

A PHASE-LOCKED LOOP (PLL) is used routinely as a variable frequency source in modern radio transceivers. A digital frequency divider is employed within the loop to reduce the reference frequency and to provide the programmability of the synthesizer. The phase noise generated by the divider can affect the synthesizer noise performance within the PLL band, especially if a high division factor is used. In fact, the divider noise power is multiplied by the square of the division factor, when it is transferred to the PLL output.

The evaluation of the divider noise is particularly significant in the design of synthesizers for Wireless Local Area Network (WLAN) standards using the Orthogonal Frequency Division Multiplexing (OFDM). In those standards, the signal-to-noise ratio (SNR) can be heavily degraded by the integral phase noise of the frequency synthesizer [1]. Moreover, the PLL for such applications typically employ the integer-N architecture, thus featuring a high division factor. Therefore, the PLL in-band phase noise can represent the dominant term of the integral value and has to be predicted during the design process.

However, the estimation of the divider noise is not straightforward. The various noise sources in the circuit affect the zero-crossing instants of the output signal and the resultant phase noise is a random process sampled at the divider output frequency. For this reason, only time-domain simulations can predict the divider's jitter. Unfortunately, such simulations are very time-consuming and provide scarce insight in the physical processes at the basis of the jitter generation. The literature offers only empirical models for classifying and describing the phase noise of digital dividers [2], [3]. These models do not account for the relative importance of the various noise sources and, in particular, they do not identify the fundamental trade-off between noise and power dissipation. That is an important issue, since the divider can be one of the most power-hungry blocks in a PLL.

This paper proposes a physical derivation of the phase noise of a frequency divider starting from the noise associated to the circuit elements. The analysis is applied to both white and flicker noise sources. The quantitative framework is verified on two 32/33 dual-modulus prescalers integrated in a 0.35-μm CMOS process. These circuits employ the frequently adopted source-coupled logic (SCL) topology and operate up to 3 GHz. The two integrated prescalers are identical apart from a synchronizing flip-flop at the output of one of them. The experiments confirm the estimates. In particular, the reduction of noise due to the synchronizer is correctly assessed. In this design, it improves the white noise by 7 dB and the flicker noise by 15 dB.

In the rest of this paper, Section II describes the method to derive an expression of the phase noise spectrum of dividers, starting from the calculation of the time jitter. This method is applied to the SCL frequency dividers in Section III, where a closed-form expression of the phase noise in the white region is obtained. In Section IV, a formula for flicker noise is found directly in the frequency domain. The prescaler design issues along with the noise estimation are discussed in Section V and the experimental results are shown in Section VI. Section VII gives the conclusion.

II. Phase Noise Spectrum of Frequency Dividers

A frequency divider is typically implemented as an asynchronous cascade of $\div 2$-dividers, where each stage is clocked by the previous one. Therefore, the time jitter of any stage, defined as the variance of the instant t_0 of the output zero crossing, is transferred to the following stage. Moreover, each stage adds its own jitter. The jitter at the output of the chain is the quadratic sum of the jitters of each stage [2].

A common topology for the $\div 2$-divider is the one represented in Fig. 1(a), where two D-latches are connected in master/slave configuration and the output of the second latch is fed back to the D input of the first latch. The jitter at the output of this $\div 2$-divider is not affected by the noise of the first latch, since the latter has no control on the output switching. Thus, only the

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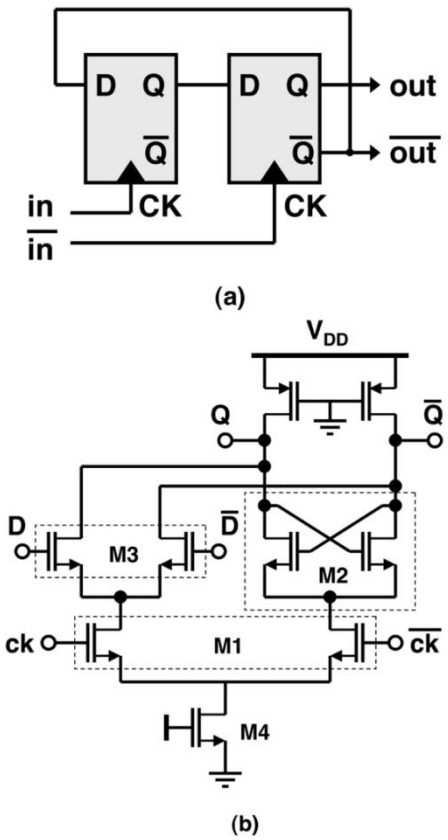

Fig. 1. (a) Block schematic of a $\div 2$-divider. (b) Circuit schematic of the D-latch in CMOS source-coupled logic.

noise sources of the second latch need to be taken into account in the evaluation of the output jitter.

The latch stage can be implemented in static [4], [5] or dynamic logic [6], [7] and the circuit can have single-ended or differential topology. In the following, we will consider static source-coupled logic (SCL) dividers as the one shown in Fig. 1(b), since they are very common in the design of dividers for gigahertz applications [8]. The pMOS transistors biased in the triode region act as load resistors. The pairs of nMOS transistors M1, M2, and M3 are alternatively switched on and off.

It is convenient to derive the phase spectrum of the latch by calculating the output jitter and then relating it to the spectrum. The time jitter can be expressed in terms of variance of the output voltage σ_V^2 as

$$\sigma_{t_0}^2 = \frac{\sigma_V^2}{(\mathrm{SL})^2} \tag{1}$$

where SL is the slope of the output voltage at the zero crossings. The period jitter (or cycle jitter) defined as the variance of the period is $\sigma_{T\,\mathrm{out}}^2 = 2\sigma_{t_0}^2$, since the period T_{out} is the difference between two subsequent switching instants.

The phase of the output signal is sampled at $f_{\mathrm{out}} = 1/T_{\mathrm{out}}$ and it is proportional to the switching instant, according to the expression $\phi = 2\pi f_{\mathrm{out}} \cdot t_0$. The sampling process folds back any noise component at frequency higher than $f_{\mathrm{out}}/2$ and the phase spectrum is defined in the Nyquist band $0 - f_{\mathrm{out}}/2$. Then, the time jitter can be written in terms of the integral of the single-sided power spectral density (PSD) of the phase S_ϕ within the Nyquist band [2], [9]

$$\sigma_{t_0}^2 = \frac{1}{4\pi^2 f_{\mathrm{out}}^2} \cdot \int_0^{f_{\mathrm{out}}/2} S_\phi(f)\, df. \tag{2}$$

For white noise, $S_\phi(f) = W$ is constant and (2) gives the link between the jitter and the phase spectrum. The single-sideband-to-carrier ratio (SSCR or $\mathcal{L}$), which is $S_\phi/2$, is

$$\mathcal{L}_{\mathrm{W}} = \frac{W}{2} = 4\pi^2 f_{\mathrm{out}} \cdot \sigma_{t_0,\mathrm{W}}^2 \tag{3}$$

The linear dependence of $\mathcal{L}_{\mathrm{W}}$ on the output frequency is in accordance with the model proposed by Kroupa [3].

In practice, even if the voltage noise spectrum is not white, the spectrum S_ϕ will result flat in the band $0 - f_{\mathrm{out}}/2$, since the sampling frequency f_{out} is usually much lower than the noise bandwidth. In the special case of $1/f$ noise, (2) leads to a diverging variance and an alternative definition of variance has to be adopted; see, for instance, [9]. However, flicker can be more conveniently treated in the frequency domain, as discussed in Section IV.

III. White Phase Noise

Although regenerative circuits typically show increased noise [10], the frequency divider at the switching instant will be shown to reduce to a simple differential pair with no positive feedback. At the zero crossings of the inputs ck, the circuit in Fig. 1(b) can be simplified as shown in Fig. 2(a), where the differential stage M1 is balanced. For a proper operation of the divider, the D signals of the second latch have already switched completely before ck starts to switch. Therefore, one of the transistors M3 is off and the other one is in triode region. The same happens to the transistors M2. Neglecting the transistors' on-resistance, the circuit can be further simplified as shown in Fig. 2(b). The p-MOSFETs have been substituted by two resistors R_L. The capacitor C_L represents the total output capacitance, given by the transistors connected at the output nodes and by the interconnect capacitance.

From the schematic in Fig. 2(b), we can simply estimate the time delay t_0 between the input clock switching and the zero-crossing instant of the differential signal $(V_{\mathrm{out}} - V_{\overline{\mathrm{out}}})$. Since both the transients of V_{out} and $V_{\overline{\mathrm{out}}}$ are exponential waveforms with the same time constant $R_L C_L$, it results that $t_0 = R_L C_L \ln 2$. It is interesting to note that any noise affecting the output nodes is band-limited by the $R_L C_L$ parallel network. Thus, the noise fluctuations are slower than the output rise or fall time and cannot trigger multiple commutations of the following stage.

The noise sources affecting the output zero crossings are also represented in Fig. 2(b). In practice, at the clock switching only one of the transistors M2 and one of M3 is on and well degenerated. Therefore, the noise sources considered are only those ones of a differential stage: the thermal noise of the pMOS loads, the noise of tail current I_B, and the noise of the nMOS transistors M1.

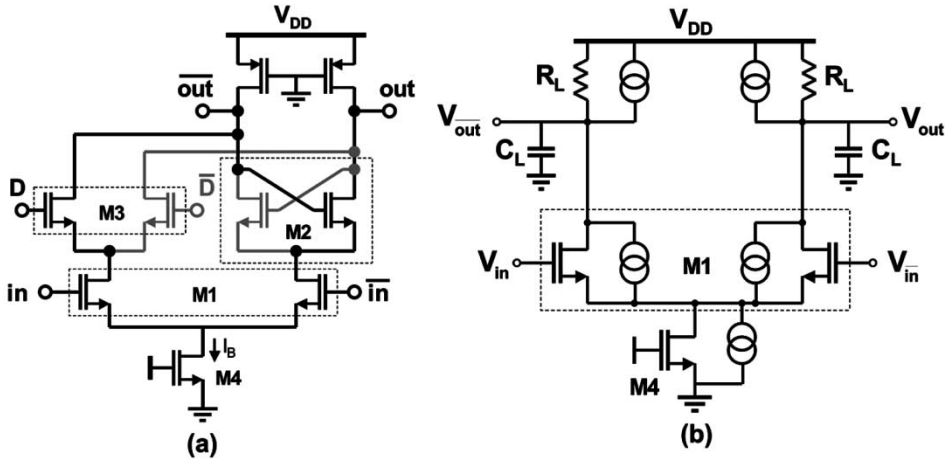

Fig. 2. (a) Schematic of the latch in Fig. 1(b) at the switching instant. (b) Simplified schematic of the same circuit with noise sources.

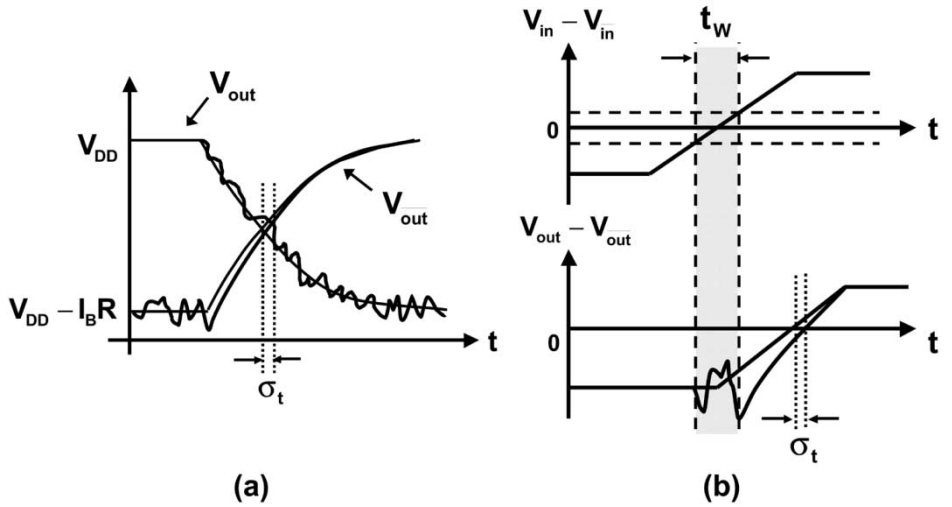

Fig. 3. Time-domain noise analysis: (a) Output voltage waveforms affected by the tail current noise. (b) Input and output differential voltage affected by the differential pair noise.

A. Load Transistors

The thermal noise of the resistors R_L causes voltage noise at the differential output $(V_{\rm out} - V_{\overline{\rm out}})$, whose variance is $\sigma_V^2 = 2kT/C_L$. The slope of the waveform $(V_{\rm out} - V_{\overline{\rm out}})$ at the zero crossings is $\mathrm{SL} = I_B/C_L$, where I_B is the bias current of M4. The resulting jitter is, therefore

$$\sigma_{t_0,\mathrm{LOAD}}^2 = \frac{2kTC_L}{I_B^2} \tag{4}$$

which can be also seen as the ratio between the power of the capacitors' charge noise $(2kT \cdot C_L)$ and the square of the bias current.

B. Tail Current Generator

The tail current generator M4 represents another noise source in the circuit of Fig. 2(b). Its current noise is alternatively injected into the nodes out and $\overline{\rm out}$. However, the effect of this noise on the outputs is different. The approach proposed in [11] for ring oscillators can be applied. Before the beginning of the transients, one of the outputs is at $V_{\rm DD}$ and the other one is at $(V_{\rm DD} - I_B R_L)$, as shown in Fig. 3(a). Only the output at the lower voltage is affected by noise. The noise variance can be obtained by multiplying the voltage spectral density $S_{I_B} R_L^2$ by the noise equivalent bandwidth $1/4R_LC$: $\sigma_V^2 = S_{I_B} R_L/4C_L$, where S_{I_B} is the single-sided PSD of the tail white noise.

The tail noise is not injected into the load during the pull-up transient, thus its variance decreases exponentially starting from the clock switching instant $(t = 0)$. The variance at time t of the voltage superimposed to the signal during the pull-up is analytically derived in the Appendix and it results that

$$\sigma_{V_{\rm up}}^2(t) = \sigma_V^2 \cdot e^{-2t/R_LC_L} \tag{5}$$

After $t = 0$, the tail noise flows toward the other output, which is pulled down. This current noise generates voltage noise whose variance increases as shown in Fig. 3(a). The variance during the pull-down transient is also derived in the Appendix and it results that

$$\sigma_{V_{\rm down}}^2(t) = \sigma_V^2 \cdot [1 - e^{-2t/R_LC_L}] \tag{6}$$

This variance tends to σ_V^2, which is the initial value of the variance in the pull-up transient. The two random processes described by (5) and (6) are uncorrelated. Even if each process

originates from the same white source, it is filtered for a different nonoverlapping time interval. The first one derives from the noise filtered between minus infinity and the clock switching, while the second one between the clock switching and t (see Appendix). It follows that the variance of $(V_{\rm out} - V_{\overline{\rm out}})$ is obtained as $\sigma^2_{V_{\rm up}} + \sigma^2_{V_{\rm down}}$. Using (5) and (6), we get $\sigma^2_V(t) = (\sigma^2_{V_{\rm up}} + \sigma^2_{V_{\rm down}}) = \sigma^2_V$, which states that the variance of the differential voltage is independent on time and equal to σ^2_V. Taking into account (1), the expression of σ^2_V and the voltage slope I_B/C_L at zero crossing, the jitter due to the tail generator noise can be written as

$$\sigma^2_{t_0,\rm TAIL} = \frac{S_{I_B} R_L}{4C_L} \cdot \frac{1}{(I_B/C_L)^2} = \frac{1}{4} \cdot \frac{4kT\gamma_T g_{d0T}}{I_B^2} \cdot R_L C_L = \frac{kT\gamma_T g_{\rm mT}}{I_B^2 \alpha_T} \cdot R_L C_L \tag{7}$$

where γ_T and g_{d0T} are respectively the noise factor and the MOS drain-source conductance at zero $V_{\rm DS}$ of the tail transistor [12]. In (7), g_{d0T} is expressed as $g_{d0T} = g_{mT}/\alpha_T$, where g_{mT} is the transistor transconductance and α_T is a constant less than one for short-channel MOSFETs [12].

C. Input Differential Pair

The channel thermal noise of the transistors M1 causes additional jitter at the output of the latch. Fig. 3(b) sketches the transients of the input and output differential signals. For simplicity, the exponential waveforms have been approximated by piecewise linear waveforms with constant slope.

When the stage is balanced [dashed area in Fig. 3(b)], both of the transistors M1 are on. This time window duration is indicated as t_W. Denoting as i_n the fluctuation of the current in one of the transistors M1, $i_n/2$ is the current perturbation injected into the load. Instead, when the input signal switches completely the differential pair, none of the transistors contributes to noise. One of them is on, but in principle fully degenerated by the current generator M4, while the other one is off. As a result, noise is injected into the load only when the input waveform is within the linear range of operation of the differential stage. The variance of the voltage noise increases exponentially during the time window t_W and tends to an asymptotic value σ^2_V. Accounting for the noise of both transistors M1, it results $\sigma^2_V = 2\cdot(kT/C_L)\cdot\gamma\cdot R_L\cdot g_m/\alpha$, where γ, g_m, and α are relative to the transistors of the differential pair. Now, an expression analogous to (6) applies and, at time t_W, it is $\sigma^2_V(t_W) = \sigma^2_V\cdot[1-e^{-2t_W/R_L C_L}]$. After the time window, the voltage noise sampled in C_L at t_W decays exponentially $\sigma^2_V(t > t_W) = \sigma^2_V\cdot[1-e^{-2t_W/R_L C_L}]\cdot e^{-2t/R_L C_L}$, according to (5). The latter expression can be approximated for $t_W \ll R_L C_L$, which holds true if the voltage swing of the waveforms is larger than the linear range of the differential stage. The variance evaluated at the zero-crossing instant $t_0 = R_L C_L \cdot \ln 2$ is $\sigma^2_V(t_0) \approx \sigma^2_V \cdot (t_W/2R_L C_L)$. Combining the expression of $\sigma^2_V(t_0)$ and (1), we get the time jitter

$$\sigma^2_{t_0,\rm DIFF\cdot PAIR} \approx \frac{kT\cdot\gamma g_m}{I_B^2\alpha}\cdot t_W. \tag{8}$$

Equation (8) can be further simplified deriving t_W from the nonlinear characteristic of the differential stage. If the transistors M1 work in velocity saturation, their transconductance is $g_m = I/V_{\rm OV}$, where I is the transistors' bias current and $V_{\rm OV}$ is the overdrive voltage. Moreover, the linear range of the differential pair is wider than $2\sqrt{2}\cdot V_{\rm OV}$ [13] and can be approximated to $4\cdot V_{\rm OV}$. The expression of the time jitter becomes

$$\sigma^2_{t_0,\rm DIFF\cdot PAIR} \approx \frac{kT\cdot\gamma g_m}{I_B^2\alpha}\cdot\frac{4V_{\rm OV}}{I_B/C_L} = \frac{2kTC_L}{I_B^2\alpha}\gamma. \tag{9}$$

D. Total Phase Noise

The total jitter is obtained from the three noise contributions of (4), (7), and (9). The correspondent phase noise level follows from (3) and it is

$$\mathcal{L}_{\rm W} = 8\pi^2\cdot\left(1+\frac{\gamma}{\alpha}+\frac{\gamma_T g_{m_T} R_L}{2\alpha_T}\right)\cdot\frac{kTC_L}{I_B^2}\cdot f_{\rm out}. \tag{10}$$

IV. Flicker Phase Noise

The analysis based on jitter cannot be easily applied to flicker noise sources. In this case, it is convenient to operate in the frequency domain. The output voltage noise at frequency $(kf_{\rm out} \pm f_m)$ (with $k = 0, 1, \ldots$ and $f_m < f_{\rm out}/2$) can be represented as a tone with amplitude V_m and random phase. Because of sampling, this voltage tone causes a phase tone at f_m, whose amplitude can be calculated as $\phi_m = 2\pi f_{\rm out}\cdot V_m/({\rm SL})$ with SL the slope at the zero crossing. Hence, the phase spectrum can be written as

$$\mathcal{L}(f_m) = \frac{2\pi^2 f^2_{\rm out}}{({\rm SL})^2}\cdot S_V^{\rm folded}(f_m) \tag{11}$$

where $S_V^{\rm folded}(f_m)$ is the PSD of the output voltage noise folded in the Nyquist band from 0 to $f_{\rm out}/2$.

In the case of white noise, (11) is equivalent to (3) since $S_V^{\rm folded}(f_m) = \sigma^2_V/(f_{\rm out}/2)$ and $\sigma^2_V = ({\rm SL})^2\cdot\sigma^2_{t_0}$. However, (11) is more general, because it allows treating also the case of flicker noise. If the corner frequency of the voltage spectrum is lower than $f_{\rm out}/2$, the flicker component undergoes no folding and $S_V^{\rm folded}(f_m)$ in (11) can be substituted by the unfolded spectrum $S_V(f_m)$. As a result, the phase noise in the flicker region is proportional to the square of the output frequency $f_{\rm out}$. This dependence has been experimentally verified in [3].

Equation (11) can be used to estimate the phase noise of a frequency divider in the flicker region, once the PSD of the output voltage $S_V(f)$ has been expressed in terms of the noise sources.

A. Tail Current Generator

Let us apply this methodology to the flicker noise coming from the tail generator. The phase spectrum depends on the sampled output voltage, as discussed in Section III. Thus, we can represent equivalently the circuit as the system in Fig. 4(a). The tail noise is fed into a suitable time-variant linear filter between the tail current and the output differential voltage, followed by a sampler at $t_0 + nT_{\rm out}$, with $n = 0, 1, \ldots$. The filter output at the zero crossings $(t_0 + nT_{\rm out})$ is equal to the voltage perturbation caused in the complete circuit at the same instants.

The function $z(t,\tau)$ derived in the Appendix is the so-called weighting or memory function of a time-variant system [14]. It provides the voltage at time t after a current impulse occurring

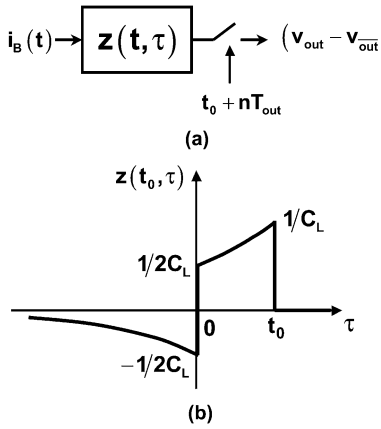

Fig. 4. Frequency domain noise analysis. (a) Equivalent system used to derive the phase noise due to the tail current noise. (b) Weighting function of the equivalent system.

at time τ. Since the output of the equivalent system is sampled at $t_0, z(t,\tau)$ has been evaluated at the zero crossing ($t = t_0$) and plotted in Fig. 4(b).

In the frequency domain, the transfer function between the tail current and the voltage before the sampling operation is the squared magnitude of the Fourier transform of $z(t_0,\tau)$ as a function of τ. This results in

$$|Z(f)|^2 = \frac{4R^2 \sin^2(\pi \cdot \ln 2 \cdot R_L C_L \cdot f)}{1 + (2\pi \cdot R_L C_L \cdot f)^2}. \tag{12}$$

The voltage spectrum is obtained by shaping the tail noise spectrum $S_{I_B}(f)$ by means of $|Z(f)|^2$ [plotted in Fig. 5(a)] and then folding the resultant spectrum in the bandwidth $f_{\rm out}/2$. The transfer function in (12) is zero at integer multiples of $f \approx 1/(\ln 2 \cdot R_L C_L)$. In particular, the tail noise near dc (like the flicker one) has no effect on the output.

This result can be intuitively understood. A low-frequency tail noise can be viewed as a static variation ΔI_B of the bias current. The effect of this perturbation is sketched in Fig. 5(b). The dashed line represents the unperturbed case, while the solid line refers to the perturbed case. The lower rail of the output increases by $\Delta I_B R_L$, but the crossing point of the two waveforms occurs at the same instant t_0 and no jitter is produced. It may seem obvious since a differential stage is known to be insensitive to common-mode noise. However, if the frequency tone becomes comparable to the inverse of the transient time (i.e., $R_L C_L \cdot \ln 2 \approx 0.7 \cdot R_L C_L$), this noise cancellation does not occur.

In practice, however, residual upconversion of flicker noise exists. Low-frequency tail noise causes amplitude noise, which can be converted into phase noise by nonlinear capacitances.

B. Input Differential Pair

While the flicker noise coming from the tail causes no jitter at the output, the flicker noise of the differential pair does produce jitter. It can be calculated by representing this noise as a voltage generator in series to the gate of the MOS transistors, whose spectrum is $S_{V_{\rm in}}(f) = K_f/f$. We assume that this noise is unaffected by the switching of the differential pair, even though some influence of the periodic transistor switching on flicker noise has been experimentally demonstrated at low switching

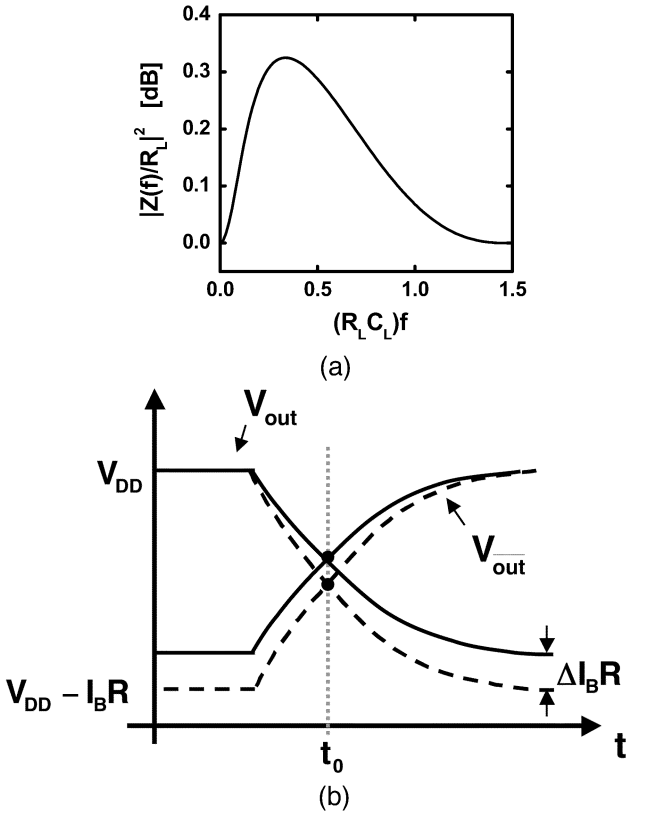

Fig. 5. (a) Transfer function of the system in Fig. 4. (b) Output voltage waveforms: unperturbed (dashed lines) and perturbed (solid lines) by a static variation ΔI_B of the tail current.

rates [15]. This low-frequency input noise can be regarded as a static perturbation $\Delta V_{\rm in}$, which alters the threshold level of the stage. Consequently, the zero crossings of the input and the output shift by the same quantity $\Delta V_{\rm in}/{\rm SL}$. The phase noise spectrum can be written as

$$\mathcal{L}_{\rm F}(f) = 2\pi^2 f_{\rm out}^2 \cdot \left(\frac{C_L}{I_B}\right)^2 \cdot \frac{2K_f}{f}. \tag{13}$$

V. Prescaler Design

The proposed phase noise analysis has been applied to the design of two 32/33 prescalers in a 0.35-μm CMOS technology with 3-V voltage supply. The two circuits only differ for the presence of a final synchronizing flip-flop. In this section, some design choices improving the divider maximum frequency are reviewed. Then, the noise considerations are applied to the design.

A. Speed Enhancement

The block schematic of the prescaler without synchronizer is drawn in Fig. 6(a). The critical condition for speed occurs when the $N/N+1$ prescaler is supposed to divide by $N+1$. The division by 33 is obtained by means of an input $2/3$-divider, which is forced to divide by 3 once every 32 input transitions by the signal MC. If the delay between the output of the $2/3$-divider and MC is higher than one clock period, the circuit cannot perform the correct division. In order to minimize this delay and to increase the maximum operating frequency, MC is provided

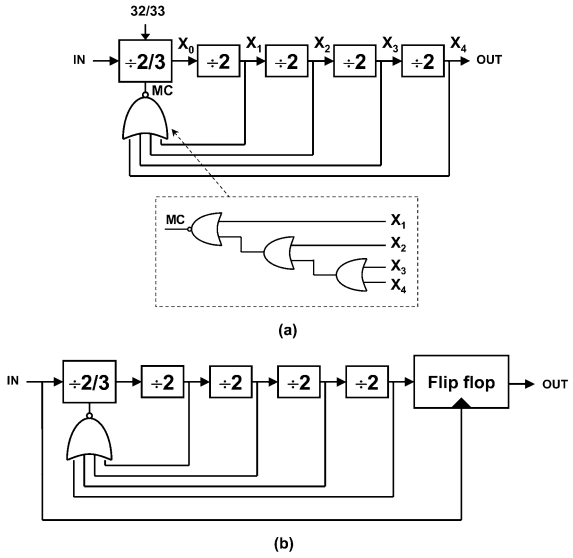

Fig. 6. Block schematic of the 32/33 prescaler: (a) nonsynchronized (NOR schematic in the inset) and (b) synchronized case.

by a NOR gate and not by an AND gate. The AND would raise MC when its inputs switch from $X_4X_3X_2X_1 = 0000$ to 1111. The MC delay would be the sum of four $\div 2$-dividers' delays plus the AND delay. Choosing a NOR gate, MC is high when its inputs switch from 0001 to 0000. Thus, the MC delay is only one divider delay plus the NOR delay. Circuit simulations show that this different architectural choice improves the maximum operating frequency from 1 to 3 GHz, in a 0.35-μm CMOS technology. Following the same principle, the implementation of the NOR gate has been optimized. Realizing the 4-inputs gate as shown in the inset in Fig. 6(a), the delay between X_1 and MC (which represents the critical path in the divider) is minimized.

B. Low-Phase-Noise Design

The presence of interconnection stray capacitances requires a minimum bias current of the latches to be able to operate at high frequency. In order to guarantee a correct operation of the prescaler up to 3 GHz over process and temperature variations, the SCL latches of the $2/3$-divider requires a minimum current I_B of 750 μA. The differential peak voltage is limited to 1 V by the voltage headroom. The load capacitance C_L is 114 fF, including the interconnection capacitance given by post-layout extraction.

The second divider stage has an input frequency of at most 1.5 GHz, thus the speed requirements of this stage are relaxed and its power consumption can be reduced. This is obtained by biasing the latches at $I_B = 250$ μA and maintaining the voltage peak at 1 V. Obviously, the transistor widths are scaled down by a factor of 3. The resultant load capacitance C_L is 55 fF, so that the waveform slope is almost halved. This scaling could be repeated theoretically at each following stage. However, since the white noise scales with the factor (C_L/I_B^2) [see (10)], the last stage would deteriorate the overall prescaler noise. For this reason, the bias current of the following $\div 2$-dividers has not been scaled further.

The jitter accumulation is the fundamental disadvantage of asynchronous dividers, but it can be easily overcome by using a synchronizing flip-flop at the end of the chain [see Fig. 6(b)] [16], [17]. In this case, the output jitter is only the one generated by the synchronizer. Since the latter works at full clock rate, its latches were sized as those in the $2/3$-divider. Adopting the synchronizer, the power consumption of the cascaded dividers can be progressively scaled down, so that a better trade-off between noise and power is achieved.

C. Noise Estimation

The equations derived in Sections III and IV have been applied to the jitter estimation of both designed dividers. The noise of the prescaler with synchronizer is only due to the last flip-flop, which has bias current $I_B = 750$ μA. According to the technology models, the transistors in the differential pair feature a noise factor $\gamma \cong 1$, while the constant $\alpha \cong 0.6$. Instead, the long-channel approximation ($\gamma_T = 2/3$ and $\alpha_T = 1$) holds true for the tail transistor. Assuming an input frequency of 2.5 GHz, the output frequency is about 78 MHz. Thus, applying (10), the estimated phase noise $\mathcal{L}_{\rm W}$ is -168 dBc/Hz.

As discussed in Section IV, the main contribution to flicker noise comes from the transistor pair. The flicker noise constant of the transistors M1 (whose aspect ratio is $9/0.35$) is $K_f = 1.4 \cdot 10^{-9}\mathrm{V}^2$. Thus, applying (13), we can estimate the flicker noise component. $\mathcal{L}_{\rm F}$ results -151 dBc/Hz at 10 kHz offset from the 78-MHz output carrier.

The estimation of the phase noise of the nonsynchronized prescaler has to take into account all the cascaded stages. The contribution of the first stage (i.e., the $2/3$-divider) is identical to the one calculated for the synchronizer. The contribution of the following $\div 2$-dividers is higher, since their latches are biased at lower current (250 μA). From (10), it follows that each one of $\div 2$-dividers contributes to the phase spectrum for -162 dBc/Hz. Summing the contributions of the 5 stages, we obtain an overall phase noise of -156 dBc/Hz.

The flicker noise of the transistor pair is also higher in the $\div 2$-dividers because of the lower bias current. Applying (13) to a single $\div 2$-divider and referring the noise to the 78-MHz output frequency, we get an estimation of $\mathcal{L}_{\rm F}$ of -148 dBc/Hz at 10 kHz. Each one of the four $\div 2$-divider contributes for the same amount to the output flicker noise. Thus, the overall flicker noise at the output is expected to be -141 dBc/Hz at 10 kHz.

VI. Experimental Results

The two 32/33-prescalers have been integrated in STMicroelectronics 0.35-μm CMOS process. A chip photograph is shown in Fig. 7. The output waveform is plotted in Fig. 8 for a 2.5-GHz input sinusoid with 50-mV peak. Both circuits work properly up to 3 GHz. The measured power dissipation is 22.5 mW and 27 mW for the nonsynchronized and the synchronized prescaler, respectively. The power consumption of the cascade of three CMOS inverters used as output buffers is not included.

The phase spectrum of the dividers cannot be measured directly at the spectrum analyzer. The phase noise introduced by the input sinusoid is some orders of magnitude higher than the divider noise, even using a high-quality frequency source. The experimental set-up in Fig. 9 circumvents this problem [2], [18].

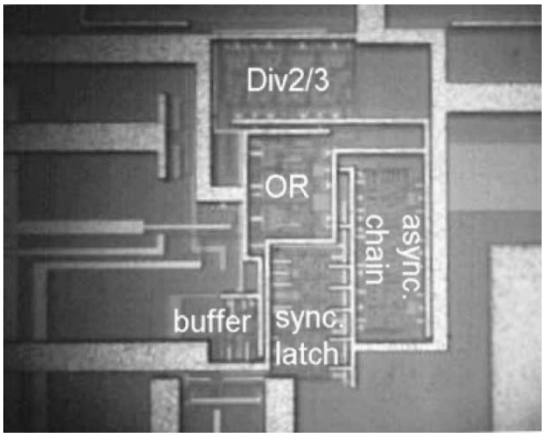

Fig. 7. Chip photograph of the synchronized 32/33 prescalers.

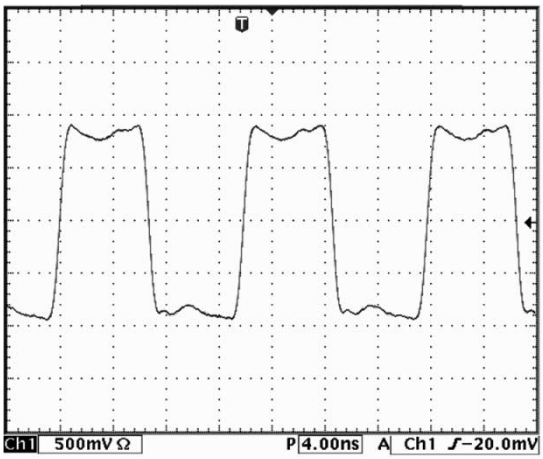

Fig. 8. Measured output voltage with 50-mV-peak input signal at 2.5 GHz.

Two identical devices are driven by the same reference and the relative phase shift between the outputs is detected by a mixer, which acts as phase detector. The reference noise is cancelled out, while the one introduced by the dividers appears downconverted at baseband. The measured spectra are shown in Fig. 10 (black lines). Note that the spectrum region from 100 Hz to 100 kHz has been measured by an FFT analyzer, while the region from 100 kHz to 10 MHz by an analog spectrum analyzer. The measured spectra are well fitted by the estimated one, shown as gray lines in Fig. 10. Only the measured noise floor of the synchronized prescaler is few dBs higher than the expected one. This is probably due to the noise added by the output buffer.

The phase noise floor of -163 dBc/Hz in the white region is remarkably good considering the low power dissipation. The device performances are summarized in Table I, together with other realizations reported in literature. While the prescaler in [19] employs dynamic logic, the phase switching technique is used in [18] and [20]. The noise floors and the $1/f$ noise corners are normalized to an output frequency of 78 MHz, using the linear dependence on $f_{\rm out}$ for the white noise and the quadratic dependence on $f_{\rm out}$ for the flicker noise.

Since the phase noise is dependent on the power consumption, it should be normalized to it. Equation (10) can be simplified noting that the time constant R_LC_L is dependent on the

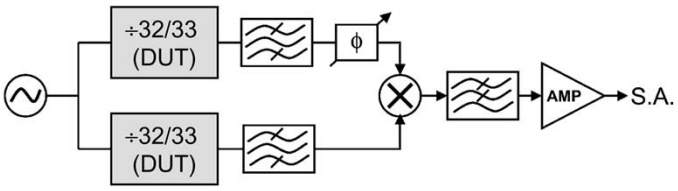

Fig. 9. Setup to measure the divider phase noise.

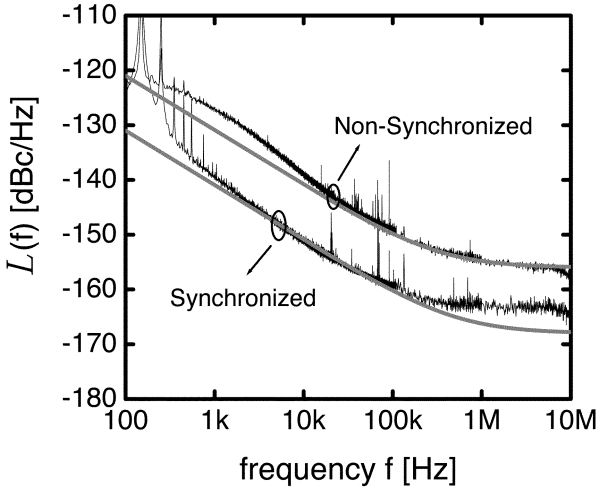

Fig. 10. Measured phase noise spectrum of the two prescalers (black lines) and estimated spectrum (gray lines).

output frequency. Higher frequency requires short transients. In particular, R_LC_L should be sufficiently lower than $1/f_{\rm out}$ to guarantee a correct operation and (10) reduces into

$$\mathcal{L}_{\rm W} = 8\pi^2 \cdot \left(1 + \frac{\gamma}{\alpha} + \frac{\gamma_T g_{m_T} R_L}{2\alpha_T}\right) \cdot \frac{kT}{P} \cdot \frac{V_{\rm DD}}{V_{\rm PEAK}} \cdot K \quad (14)$$

where P is the dissipated power from the voltage supply $V_{\rm DD}, V_{\rm PEAK}$ is the peak of the differential output and $K = 1/(f_{\rm out}R_LC_L)$ is a speed margin factor. Thus, phase noise can be traded against the dissipated power and an appropriate figure of merit (FoM) can be defined as the inverse of the phase noise-power product $\mathrm{FoM} = 1/(\mathcal{L}_{\rm W} \cdot P)$. The power consumption is expressed in milliwatts and it is normalized to the number of stage of the $N/N+1$-divider, which is $1 + \log_2(N)$. The values of the FoM are reported in Table I.

VII. Conclusion

This paper has shown a physical derivation of the phase noise of frequency dividers. This analysis takes into account both white and flicker noise sources and it is verified on two SCL 32/33-prescalers integrated in a 0.35-μm CMOS process. The two prescalers are identical apart from a synchronizing flip-flop at the output of one of them. The measured phase spectra are in well agreement with the estimates. The final synchronization improves the white noise by 7 dB and the flicker component by 15 dB. The maximum operating frequency is 3 GHz, the power consumption is 27 mW and the phase noise floor is -163 dBc/Hz. The existence of a tradeoff between phase noise and power consumption has been demonstrated.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER PUBLISHED DUAL-MODULUS DIVIDERS

Ref.	N/N+1	Maximum input frequency	Noise Floor $\mathcal{L}_W$ (f_{out} = 78 MHz)	Power	FoM	Flicker Corner Frequency	Technology
[20]	128/129	1.75 GHz	-133 dBc/Hz	24 mW	128 dB	70 kHz	0.7μm-CMOS
[18]	220/224	5.5 GHz	-148 dBc/Hz	59 mW	139 dB	300 kHz	0.25μm-CMOS
[19]	8/9	1.5 GHz	-167 dBc/Hz	55 mW	156 dB	800 kHz	0.7μm-CMOS
This work	**32/33**	**3 GHz**	**-163 dBc/Hz**	**27 mW**	**156 dB**	**200 kHz**	**0.35μm-CMOS**

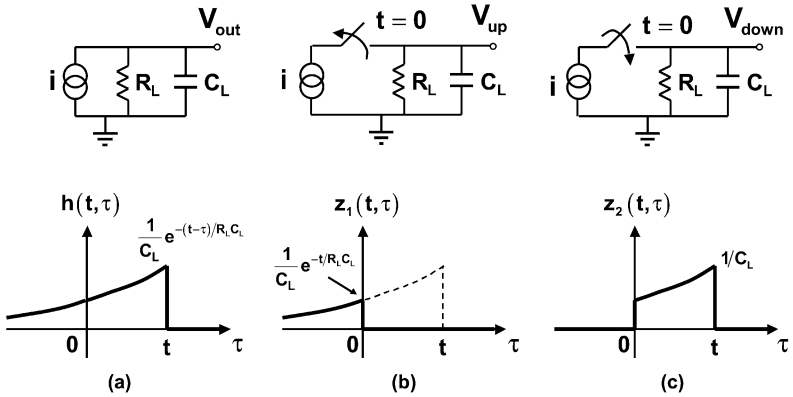

Fig. 11. Circuits and respective weighting functions discussed in the Appendix. (a) Standard *RC* filter. (b) Latch output during the pull-up transient. (c) During the pull-down transient.

APPENDIX

In this Appendix, the variances of the output voltages of the circuit in Fig. 2(b), due to the tail current noise, are derived. We analyze separately the effect of noise on the pull-up and on the pull-down transients. To make the following analysis clearer, it is useful to recall the behavior of the circuit in Fig. 11(a). Being a linear system, the voltage output at time t can be written as $V_{\rm out}(t) = \int_{-\infty}^{t} i(\tau)h(t,\tau)\,d\tau$, where $i(\tau)$ with $\tau < t$ is the current signal. The function $h(t,\tau)$ shown in Fig. 11(a) is called weighting or memory function [14], because it provides the contribution of the current unit impulse at instant τ to the voltage at t. Since this system is time-invariant, the previous integral can be seen as the convolution product between $i(\tau)$ and the circuit impulse response.

The circuit in Fig. 2(b) has instead a time-variant transfer for the tail noise. We assume that the differential stage acts as a hard switching. Thus at $t = 0$, the whole bias current is instantaneously steered from one transistor into the other one. Correspondently, the tail noise is injected into one of the outputs load for $t < 0$ and in the other one for $t > 0$. Therefore, it is convenient to study separately the effect of the tail noise on the output that is pulled up ($V_{\rm up}$) and on the one that is pulled down ($V_{\rm down}$).

The shape of the weighting function $z_1(t,\tau)$ referred to the first output is shown in Fig. 11(b). When $t < 0$, $z_1(t,\tau)$ is identical to $h(t,\tau)$. When $t > 0$ [case represented in Fig. 11(b)], the function is windowed and the dashed part is missing, because a current impulse injected at any $\tau > 0$ has no effect on $V_{\rm up}$. Moreover, as t increases, the weight of a current impulse at $\tau < 0$ reduces. That accounts for the exponential discharge of the voltage sampled on C_L.

The very same discussion holds for the function $z_2(t,\tau)$, referred to the output that is pulled down and shown in Fig. 11(c). For $t < 0$, the function is zero, since the current generator is not connected to the circuit in Fig. 11(c). For $t > 0$ [case represented in Fig. 11(c)], $z_2(t,\tau)$ is the function $h(t,\tau)$ truncated to zero for $\tau < 0$. In fact, a current impulse injected at $\tau < 0$ does not reach this output. The resulting $z_2(t,\tau)$ is exactly the portion of $h(t,\tau)$ missing in $z_1(t,\tau)$.

In a time-variant system featuring a weighting function $z(t,\tau)$, we can calculate the autocorrelation function of the output signal as $R_{vv}(t_1,t_2) = \iint_{-\infty}^{+\infty} R_{ii}(\tau_1,\tau_2)z(t_1,\tau_1)z(t_2,\tau_2)\,d\tau_1\,d\tau_2$, where $R_{ii}(t_1,t_2)$ is the autocorrelation of the current noise. Assuming the current noise to be white, $R_{ii}(t_1,t_2)$ is a Dirac impulse $R_{ii}(t_1,t_2) = (S_{I_B}/2)\cdot\delta(t_2-t_1)$, where S_{I_B} is the single-sided PSD of the current noise. Hence, the variance of the output signal reduces to

$$\begin{aligned}\sigma_v^2(t) &= R_{vv}(t,t)\\ &= \iint_{-\infty}^{+\infty} (S_{I_B}/2)\cdot\delta(\tau_2-\tau_1)z(t,\tau_1)z(t,\tau_2)\,d\tau_1\,d\tau_2\\ &= (S_{I_B}/2)\cdot\int_{-\infty}^{+\infty} z^2(t,\tau)\,d\tau. \end{aligned} \tag{15}$$

Substituting the expression of $z_1(t,\tau)$ in (15), we get the variance of the output voltage during the pull-up

$$\begin{aligned}\sigma_{V_{\rm up}}^2(t) &= (S_{I_B}/2)\cdot\int_{-\infty}^{0} (1/C_L)^2 e^{-2(t-\tau)/R_LC_L}\,d\tau\\ &= (S_{I_B}R_L/4C_L)\cdot e^{-2t/R_LC_L}. \end{aligned} \tag{16}$$

Instead, using $z_2(t,\tau)$ in (15), we obtain the variance of the voltage during the pull-down

$$\sigma^2_{V_{\rm down}}(t) = (S_{I_B}/2)\cdot\int_0^t (1/C_L)^2 e^{-2(t-\tau)/R_L C_L} d\tau = (S_{I_B}R_L/4C_L)\cdot(1-e^{-2t/R_L C_L}). \quad (17)$$

Now, a weighting function $z(t,\tau)$ can be defined which describes the transfer between the tail current noise and the differential voltage of the circuit in Fig. 2(b). Noting that the output voltage is the difference between $V_{\rm out}$ and $V_{\overline{\rm out}}$, it results $z(t,\tau) = z_2(t,\tau) - z_1(t,\tau)$. This function is plotted for $t = t_0$ in Fig. 4(b). The area under $z(t_0,\tau)$ is zero, in accordance with the transfer function in Fig. 5(a), which is zero at dc. Moreover, it is now evident why the variance of the output is $\sigma^2_V(t) = \sigma^2_{V_{\rm up}} + \sigma^2_{V_{\rm down}} = S_{I_B}R_L/4C_L$, as obtained in Section III. Since it is $z^2(t,\tau) = h^2(t,\tau)$ for any $t, \sigma^2_V(t)$ is identical to the voltage variance after forcing a time-invariant parallel RC with a current white noise. Consequently, it is independent on t and it is given by $S_{I_B}R_L/4C_L$.

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